HN

# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/942,328 | 08/28/2001 | Padmanabha I. Venkitakrishnan | HP-10008019-1 | 7710 |

7590 01/10/2005

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P.O. Box 272400
Fort Collins, CO 80527-2400

| EXAMINER | |
|---|---|
| KIM, HONG CHONG | |
| **ART UNIT** | **PAPER NUMBER** |
| 2186 | |

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/942,328 | VENKITAKRISHNAN ET AL. | |
| | Examiner | Art Unit | |
| | Hong C Kim | 2186 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 11-21* is/are rejected.

7)☒ Claim(s) *3-10* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**Detailed Action**

1. Claims 1-21 are presented for examination. This office action is in response to the amendment filed on 10/19/2004.

2. The examiner requests, in response to this Office action, any reference(s) known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. This **request** is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the application's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event prior art documentation is submitted, a discussion of relevant

passages, figs. etc. with respect to the claims is requested. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, his/her discussion of the reference(s) with respect to the instant claims is essential. **A response to this inquiry is greatly appreciated.**

**The examiner also requests**, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s), in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

3. Applicants are reminded of the duty to disclose information under 37 CFR 1.56.

***Claim Rejections - 35 USC ' 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al. (Carpenter) US Patent No. 6,115,804 in view of Cherabuddi US Patent Application Pub No. 2002/0184445 .

As to claim 11, Carpenter discloses the invention as claimed. Carpenter discloses a cache coherency system comprising: a plurality of cache memories (col. 3 lines 50-51) including a cache line for storing information; a plurality of processor cores (Fig. 10's) on a single substrate for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and a coherency system bus (col. 4 lines 52+, col. 5 lines 3+, Table I (Address Modifiers defining attributes of a communication transaction for coherency, write thru, and protection) and Fig. 1 Ref. 22).) for providing coherency in accordance with a memory coherency maintenance method, wherein said memory coherency maintenance method maintains coherency throughout a shared memory model including said plurality of cache memories. However, Carpenter does not specifically disclose a plurality of processor cores on a single substrate.

Cherabuddi discloses a plurality of processor cores on a single substrate (block4) for the purpose of providing capability of parallel processing (block 4) and decreasing the size and power consumption and increasing the speed by decreasing the distance among the components.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a plurality of processor cores included on a single substrate as shown in Cherabuddi into the teaching of Carpenter thereby results in an invention as claimed.

5. Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al. (Carpenter) US Patent No. 6,115,804 in view of Parks US Patent No. 6,356,983.

As to claim 18, Carpenter discloses the invention as claimed. Carpenter discloses a cache coherency method comprising: invalidating said cache line; modifying said cache line; and sharing said cache line (Table VI). However, Carpenter does not specifically disclose pausing actions to a cache line. Parks discloses pausing actions to a cache line (col. 9 lines 55-60, cache miss, busy, and pending reads on this limitation since those states need to pause or interrupt the current action to take next action) for the purpose of maintaining data consistency.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate pausing actions to a cache line of Parks in the teaching of Carpenter thereby results in an invention as claimed.

As to claim 19, Carpenter further discloses wherein said sharing a cache line includes a sharing control process further comprises: permitting internal reading of said cache line without shared bus activity; and producing a invalid cache line transaction when said cache line is internally written (Table VI).

As to claim 20, Parks further discloses producing an internal access line miss; and causing a processor core to fetch said cache line information from a on chip system bus (OCSB) (col. 2 lines 24+).

As to claim 21, Carpenter further discloses wherein modifying said cache line produces a modified cache line state and includes a more recent value than a main memory (Table VI).

6. Claims 1-2, and 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carpenter et al. (Carpenter) US Patent No. 6,115,804 in view of Parks US Patent No. 6,356,983 and further in view of Cherabuddi US Patent Application Pub No. 2002/0184445 .

As to claim 1, Carpenter discloses the invention as claimed. Carpenter discloses a cache coherency maintenance system, comprising: a plurality of cache memories including a cache line for storing information (col. 3 lines 50-51); a plurality of processor cores (Fig. 10's) for processing instructions and information stored in said plurality of cache memories wherein one of said plurality of processor cores is coupled to and associated with one of said plurality of cache memories; and a coherency system bus (col. 4 lines 52+, col. 5 lines 3+, Table I (Address Modifiers defining attributes of a communication transaction for coherency, write thru, and protection) and Fig. 1 Ref. 22) for communicating information between said plurality of cache memories and said plurality of processor cores in accordance with a coherency protocol, wherein said coherency protocol state with said cache line. However, Carpenter does not specifically disclose a pending state. Parks discloses a pending state (col. 9 lines 55-60) for the purpose of maintaining data consistency.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a pending state of Parks in the teaching of Carpenter thereby results in an invention as claimed.

However, neither Carpenter nor Parks specifically discloses a plurality of processor cores included on a single substrate.

Cherabuddi discloses a plurality of processor cores included on a single substrate (block4) for the purpose of providing capability of parallel processing and decreasing the size and power consumption and increasing the speed by decreasing the distance among the components.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a plurality of processor cores included on a single substrate as shown in Cherabuddi into the combined teaching of Carpenter and Parks thereby results in an invention as claimed.

As to claim 2, Parks further discloses wherein said pending state locks out access to said cache line when said cache line is in transition and continues to lock out access to said cache line until appropriate responses are received indicating continuation of a cache line transaction will not result in race conditions that cause information coherency problems (col. 3 lines 1-3 and col. 9 lines 50-60).

As to claim 12, Carpenter and Cherabuddi disclose the invention as claimed. Carpenter further discloses attempting to access information in a first memory (col. 9

lines 10-12); changing to a modify state; transitioning to an invalid state; and shifting to a shared state (Table VI). However, neither Carpenter nor Cherabuddi specifically discloses a pending state. Parks discloses a pending state (col. 9 lines 55-60) for the purpose of maintaining data consistency.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate a pending state of Parks in the combined teaching of Carpenter and Cherabuddi thereby results in an invention as claimed.

As to claim 13, Parks further discloses wherein said memory coherency maintenance method comprises a pending state that locks out access to information included in one of said plurality of caches while transitioning between other states (col. 3 lines 1-3 and col. 9 lines 50-60).

As to claim 14, Parks further discloses wherein one of said plurality of processors attempts to access information from an external cache (col. 2 lines 25-28).

As to claim 15, Carpenter further discloses wherein a modified state is entered in one of said plurality of cache memories and the information is put into an invalid state in the remaining of said plurality of cache memories (Table VI).

As to claim 16, Carpenter further discloses an embedded memory for storing information and data for downloading to said plurality of cache memories and utilization by said plurality of processors (col. 4 lines 29+).

As to claim 17, Carpenter further discloses wherein said cache line is in a shared state and comprises the same value as in said embedded main memory (Table VI).

### *Allowable Subject Matter*

7. Claims 3-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

8. Applicant's arguments filed 10/19/2004 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Cherabuddi

discloses a plurality of processor cores included on a single substrate (block4) for the purpose of providing capability of parallel processing (block 4) and decreasing the size and power consumption and increasing the speed by decreasing the distance among the components.

In response to applicant's argument on page 11 that the prior arts do not disclose a coherency system bus has been fully considered but it is not persuasive.

Carpenter discloses a coherency system bus (col. 4 lines 52+, col. 5 lines 3+, Table I (Address Modifiers defining attributes of a communication transaction for coherency, write thru, and protection) and Fig. 1 Ref. 22).

***Conclusion***

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. ' 1.111(c).

12. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hong C Kim whose telephone number is 571-272-4181. The examiner can normally be reached on M-F 9:00 to 6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

14. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

**or faxed to TC-2100:**
(703) 872-9306

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

HK
Primary Patent Examiner
January 5, 2005